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# A Boundary Scan Test Vehicle for Direct Chip Attach (DCA) Testing

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# Topics

- *Background: Direct Chip Attach*

- *Test Methods*

- *What is boundary scan and how does it work*

- *How is it currently being used*

- *Usefulness to others*

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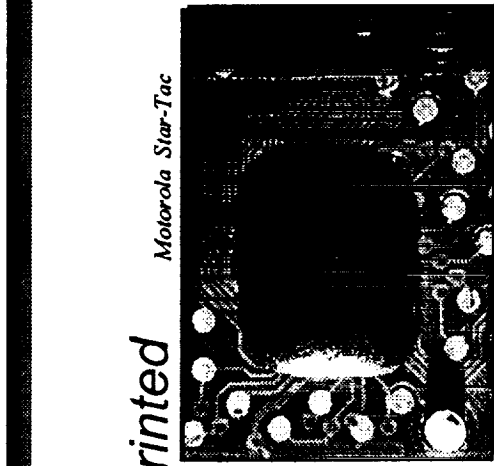# Background: What is Direct Chip Attach?

- Equivalent to Chip-On-Board
- Bare die bonded directly to the printed wiring board
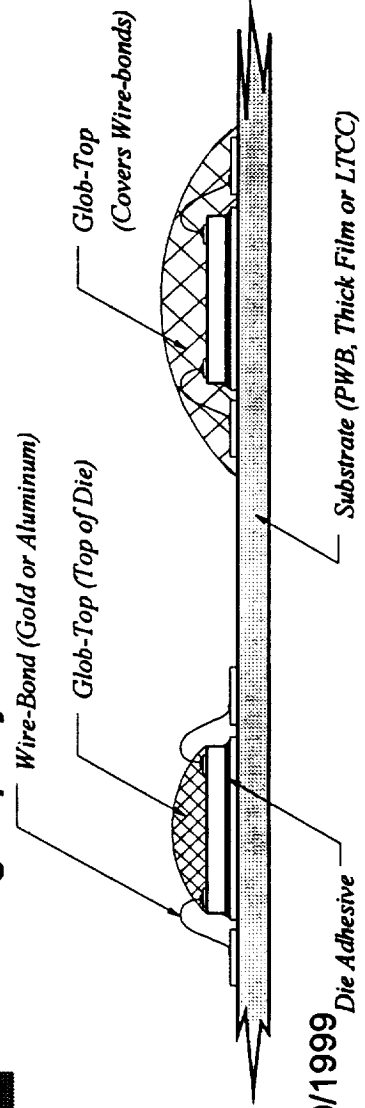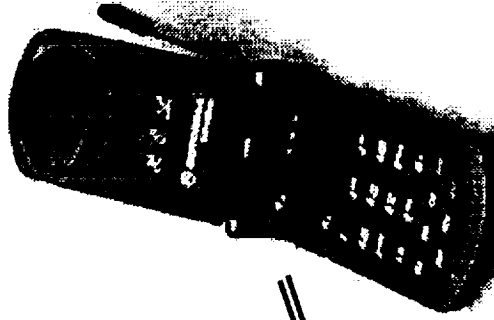- Wire bonded
- Non-Hermetic Packaging
- To validate an encapsulation or passivation technology for New Millenium Deep Space – 2 (DS-2) and other flight projects



*Motorola Star-Tac*

Ref: Binghamton University web page (http://www.iccc.binghamton.edu/iccc/)

Ref: Circuits Assembly, 1996

Wire-Bond (Gold or Aluminum)

Glob-Top (Top of Die)

Glob-Top (Covers Wire-bonds)

Substrate (PWB, Thick Film or LTCC)

Die Adhesive

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# Background:DCA Objectives

To design a substrate that

- gives a realistic understanding of how the environment affects powered devices
- provides information about the reliability of passivation technology

■ Span wide range of part types

■ Testing

- Fast
- Automated
- Repetitive
- Log data

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# Test Methods

## Daisy Chain

- simple for solder joints or connectors
- non-powered devices
- don't know exactly what interconnect has failed

## ■ Boundary Scan

- IEEE Standard (JTAG)
  - Standardized
  - Commercially available
- powered devices
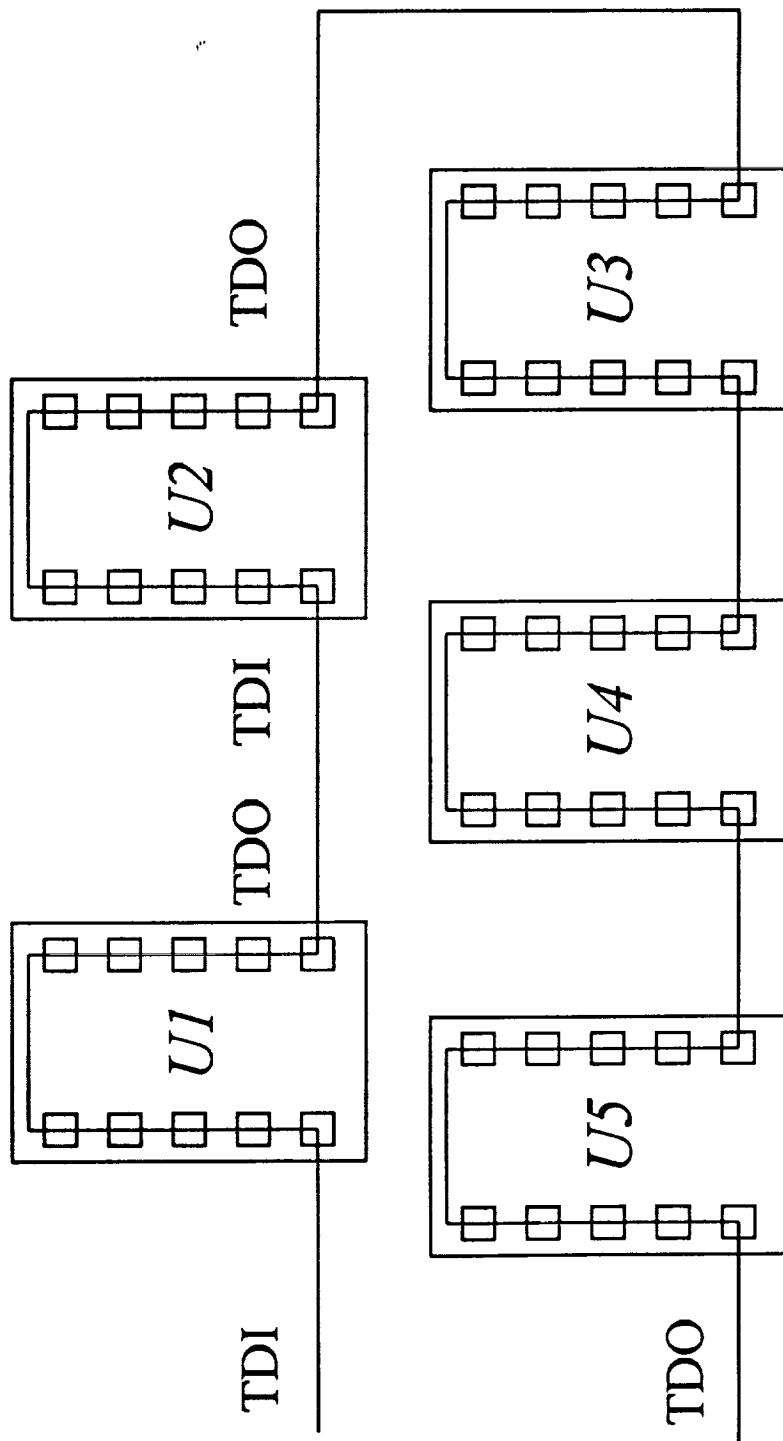- digital test
- determine failure at interconnect level
  - short
  - open

# Boundary Scan Chip



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# Board Design

Boundary Scan Devices

Mosfet

S/R Patterns

Diode

Memory Chip

Sandia Test Chip ATC2.5

Sandia Test Chip NAT01

A to D Converters

U1

U2

U3

U4

U5

TDI

TDO

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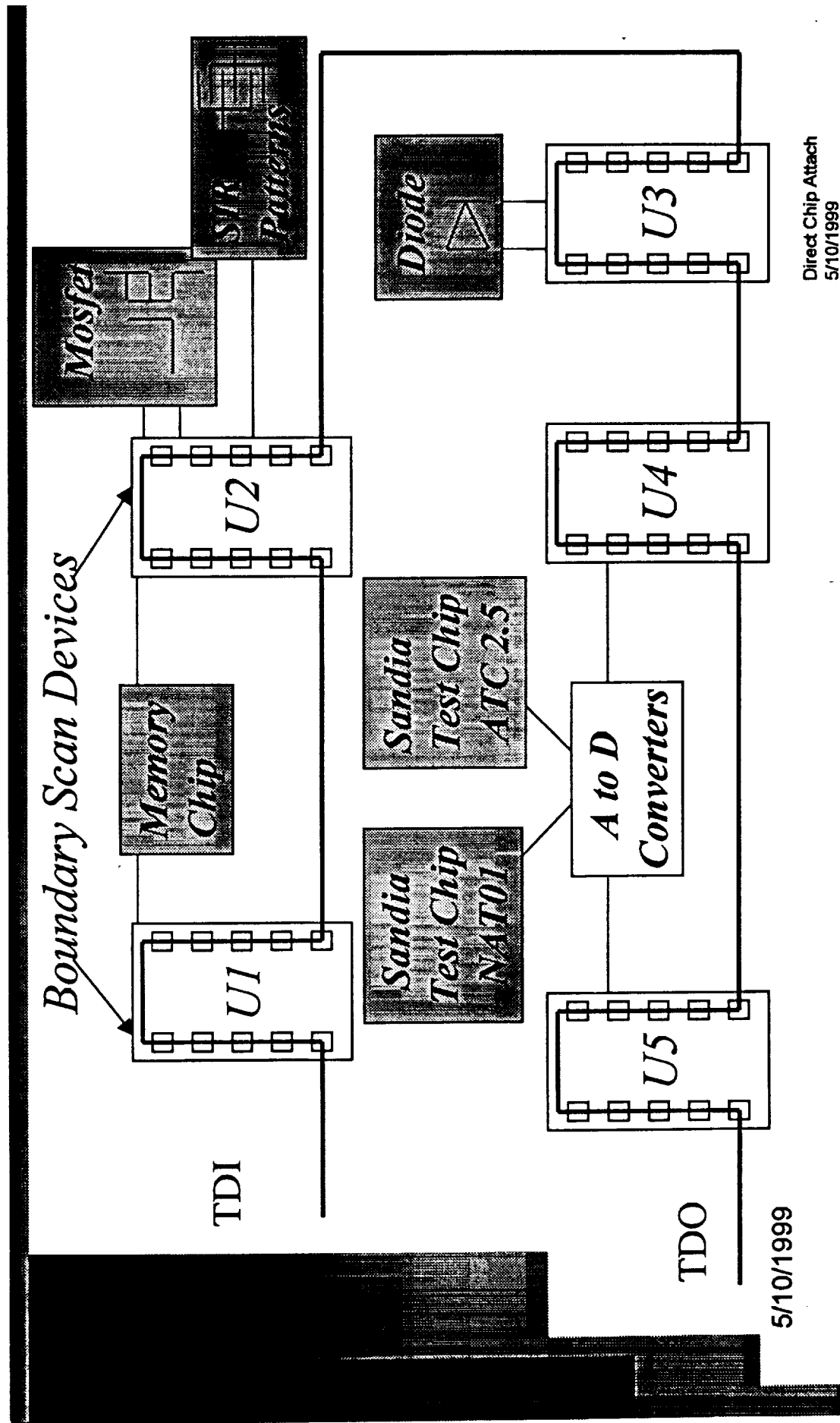
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# Devices on Board

## Packaged Parts

- Boundary Scan Chips
- Resistors
- A to D Converters

## ■ Bare Die

- A Memory Chip
- Several Schottky Diodes
- MOSFETs (Both N and P Channel)
- Sandia Test Chips
  - ATC 2.5
  - NAT01
- SIR Patterns

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# Boundary Scan Test

- Diodes – Series connected with resistor

- Mosfets – N and P channel configured as inverters

- SIR Patterns – Voltage divider will show non-zero value if current flows

- ATC2.5 / NAT01 – A to D Converters will sense change in voltage divider

# Test of Static Memory (SRAM) by Boundary Scan

## Boundary Scan used to write to SRAM

- Boundary Scan Chip 1 feeds addresses
- Boundary Scan Chip 1 feeds data inputs

## Boundary Scan used to read SRAM

- Chip 1 feeds addresses
- Chip 2 reads Data outputs

■ Data shifted out - verified

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# The Boundary Scan Scan Test System

## Asset

- ## Hardware Card

- ## Interface Pod

- ## Windows Software

**ASSET Tool Box**

File  Design  Scan Path  Interconnect  Memory  Logic  ISP  Custom  Utilities  Windows  Help

**Macros**

Apply To:  Dcabd

Hierarchy...

Source Format
- ⦿ Macro Source
- ◯ Macro Executable

Processing Stages
- ☒ Compile
- ☑ Apply

Macro Filename:  C:\ASSET23\DcaAsset\DCAbrd\Macros\Scanpth3.

Destination File:  C:\ASSET23\DcaAsset\DCAbrd\Macros\Scanpth3.

Browse...

Arguments:

Process  Save & Close  Cancel

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# The Boundary Scan Scan Test System

- Uses Macros to program test

- Compares test data out to data expected

Scan Path ATPG: Test results for entity dcabd3. This test detects:
- Stuck-at-0 on the TDI/TDO data path.
- Inoperative TCK.
- Inoperative TMS.
- Incorrect scan path length.

Pattern Is Constant 1

Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0

Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
Pattern Is Constant 0110

Step 1. Expect the value normally captured by the BYPASS/IDCODE registers.
No failures detected.
Step 2. Expect the pattern shifted through the BYPASS/IDCODE registers.
No failures detected.
INFO MAX064: C:\ASSET23\DcaAsset\DCABrd\Macros\Scanpth3.mac(247) Program ran successfully.

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# The Boundary Scan Scan Test System

## LabVIEW

- Logs time, date, and other relevant information when there is a failure

- Continuous testing



TC Selections to CHART

Panel Log to Spreadsheet File

Append  A:

Overwrite  C:

Reset Panel LOG

Re-Enable ALL Channels

Enabled

| Date | Time | Failed Ch. | Temp. | Thermcpl. | Cycles | State |
|------|------|------------|-------|-----------|--------|-------|
|      |      |            |       |           |        |       |

Total Failures on Display

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# Successfully able to test

diodes

mosfets

SRAM



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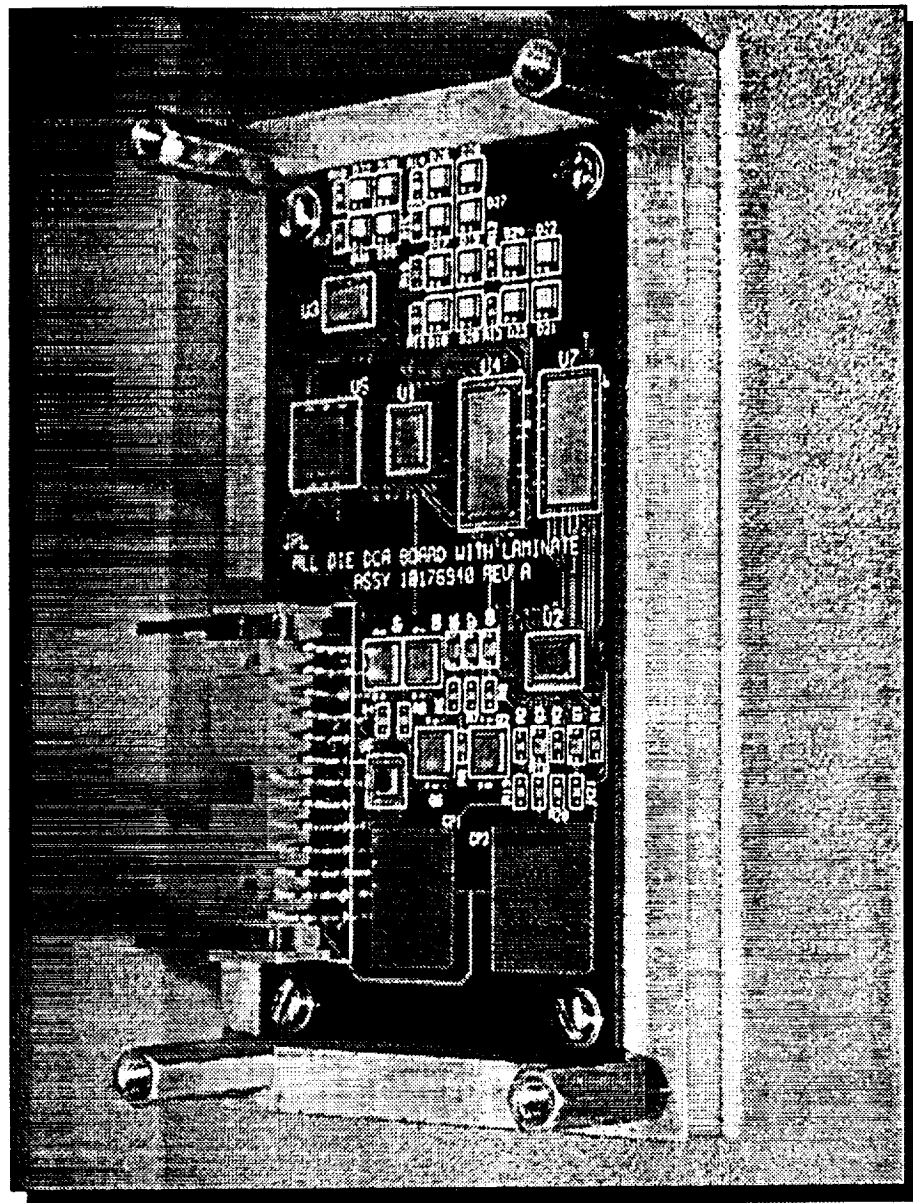
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# Future Tasks

- LabVIEW up and running
- Continuous testing in thermal and HAST chambers
- Testing all different types of new Packaging technologies

# Summary

## Boundary Scan use for DCA

- test at interconnect level
- automated testing that logs failures

## Boundary Scan as a valuable resource to testing new technologies